REMARKS

At the outset, the Examiner is thanked for the review and consideration of the pending application. The Non-Final Office Action dated November 7, 2008 has been received and reviewed. Reconsideration of the pending application is respectfully requested in view of the following observations.

1. Amendments and Support for Same.

By this Response, claims 20-22, 24, 26-34 and 36-38 are hereby amended, support for which is found throughout Applicant's Specification. No new matter is believed to be added. Claims 1-19 have previously been cancelled. Claims 23, 25 and 35 are herein cancelled; claims 39-61 are hereby newly added, support for which is found throughout Applicant's Specification. No new matter is believed added.

Claims 20-22, 24, 26-34 and 36-61 are thus pending.

2. Examiner Interview.

Examiners Slutsker and Sarkar are thanked for courtesies extended during a personal interview on January 15, 2009.

The substance of the interview is embodied in the Examiner's PTOL-413 form of January 15, 2009.

3. Claims 20, 21, 22, 27 and 28-34 are rejected under 35 U.S.C. §112(2) as indefinite.

The Examiner has rejected claims 20, 21, 22, 27 and 28-34 as indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The Examiner has rejected the above-noted claims for reasons as described in the Office Action at pages 2-4 thereof.

Applicant has amended claim 20 to include the steps of forming the intermediate layer by depositing an amorphous silicon layer and then crystallising the amorphous silicon layer to form a polycrystalline layer which is located between the high resistivity silicon substrate and the insulating layer in order to increase the charge trap density between the insulating layer and the high resistivity silicon substrate. The above claim limitations are not mere intended outcome recitations but

provide the steps which will lead to this result, see for example, Specification at pages 4-6 thereof.

Applicant has amended claim 21 to remove "preferably smaller than 50 nm."

Claim 22 is amended to remove, "at least $10^{11}/cm^2/eV$, preferably."

Applicant has amended claims 27 and 28 as noted.

Claim 29 is amended to remove, "this" and further clarification is recited.

Claim 30 has been amended to remove, "at least 100 nm, preferably between 100 nm and 450 nm, more preferred between 200 nm and 300 nm."

Applicant has amended claim 31 to remove, "after a standard CMOS process is performed on the structure."

Applicant has amended claim 32 as noted.

Claims 33 and 34 have been amended to remove, "preferably at least $10^{12}/cm^2/eV$" and "preferably higher than 10 kΩ.cm", respectively.

All of the Examiner's indefiniteness rejections are believed to be addressed.

Accordingly, withdrawal of the rejection of claims 20-22 and 27-34 as indefinite is respectfully requested.

4. Claims 20-24, 27-33 and 35-38 are rejected under 35 U.S.C. §103(a) as unpatentable over United States patent application publication 2003/0129780 A1 (*Auberton-Herve*) in view of Applicant's Admitted Prior Art (*AAPA*).

The rejection of claims 20-24 and 27-31 has been carefully considered but is most respectfully traversed and reconsideration is requested.

The combination of *Auberton-Herve* and *AAPA* does not teach or suggest all of the claim limitations and therefore does not render the claimed invention *prima facie* obvious.

Claim 20 has been amended to include limitations from claim 25.

Claim 25 was not rejected as obvious over only the combination of *Auberton-Herve* and *AAPA* and the addition of that limitation from claim 25 to claim 20 obviates the rejection.

Furthermore, the Examiner admits that "Auberton-Herve in view of AAPA does not teaches that applying a polysilicon layer comprises depositing amorphous silicon on the silicon substrate and crystallizing the amorphous silicon so as to form the polysilicon layer (Office Action at page 8)."

Therefore, the combination of *Auberton-Herve* and *AAPA* does not render the claimed invention of claims 20-24 and 27-31 *prima facie* obvious.

Withdrawal of the rejection of claims 20-24 and 27-31 is most respectfully requested.

The rejection of claims 32-33 and 35-38 has been carefully considered but is most respectfully traversed and reconsideration is requested.

Claim 32 has been amended to recite, the intermediate layer being a re-crystallized polysilicon layer.

As noted above, the Examiner recognizes that the combination of *Auberton-Herve* and *AAPA* fails to teach or suggest at least applying a polysilicon layer comprises depositing amorphous silicon on the silicon substrate and crystallizing the amorphous silicon so as to form the polysilicon layer.

Accordingly, the combination of *Auberton-Herve* and *AAPA* does not teach or suggest the claimed intermediate layer being a re-crystallized polysilicon layer.

Withdrawal of the rejection of claims 32-33 and 35-38 is most respectfully requested.

5. Claims 25 and 26 are rejected under 35 U.S.C. §103(a) as unpatentable over United States patent application publication 2003/0129780 A1 (*Auberton-Herve*) in view of Applicant's Admitted Prior Art (*AAPA*) and further in view of European patent application EP 1 014 452 A1 (*Inoue*).

The rejection of claims 25 and 26 has been carefully considered but is most respectfully traversed.

Claim 25 is cancelled but is included in claim 20 as amended.

The combination of *Auberton-Herve*, *AAPA* and *Inoue* does not render the claimed invention *prima facie* obvious because the combination does not teach or suggest all of the claim limitations. *Auberton-Herve* requires an immediate layer of

amorphous silicon for bonding an active material layer onto a face of a support and there is no motivation to convert this bonding layer to a polysilicon layer having a high trap density in accordance with the claimed invention. Furthermore, the claimed invention results in advantages not taught or suggested by the combination of *Auberton-Herve*, *AAPA* and *Inoue*.

Considering *Auberton-Herve*, the structure that is taught in *Auberton-Herve* is different from the claimed invention. *Auberton-Herve*'s approach consists of introducing an amorphous material between a first material and a second material (such as polycrystalline silicon) that is less noble than the first material. The reason for their work is to facilitate the bonding between the first and less noble materials. The intermediate layer used in *Auberton-Herve* is thermodynamically unstable (i.e. the amorphous layer will recrystallize above ~400°C in the case of Si).

In the claimed invention, the claimed amorphous layer is introduced between a monocrystalline silicon substrate and an insulator. The purpose of this intermediate layer is to electrically passivate the surface of the Si substrate. The amorphous silicon layer is then recrystallised, thereby changing its morphology from amorphous to polycrystalline, in order to produce a high density of small grains. In the claimed invention, the re-crystallisation is used to generate a layer with a high trap density as the re-crystallisation process produces many smaller crystals and hence defects that can act as traps and provides the unique characteristic of the presently claimed invention.

The resulting structure is thus different from what is taught in *Auberton-Herve*, as there is no longer an amorphous layer. The claimed intermediate layer is thermodynamically stable, i.e., it will not be affected by large temperature budgets.

Turning to *Inoue*, *Inoue* relates to thin-film devices in particular to transferring thin-film devices. Although *Inoue* discusses converting an amorphous silicon layer into a polysilicon layer, this is for a different purpose from that which is claimed in the present invention. In order to make large size display devices, amorphous silicon deposition is advantageous in that it is almost independent of size whereas the use of wafers of monocrystalline silicon is limited in size. Hence, *Inoue*'s re-crystallisation is used to generate a silicon layer that can be used to make a (what may be a poor quality) transistor.

Thus, the claimed invention provides the advantage of a method of manufacturing multilayer semiconductor structures and multilayer semiconductor structures suitable for use in high frequency applications. The claimed invention results in ohmic losses that are as low as possible in order to prevent deterioration of the electrical performance of the multilayer structure in particular for high frequency applications.

Auberton-Herve is directed to manufacturing substrates in which an active material element is transferred onto a support including bonding an active layer onto a support and problems associated with control of polishing. Auberton-Herve has nothing to do with manufacturing multilayer semiconductor structures and multilayer semiconductor structures suitable for use in high frequency applications. As noted, *Auberton-Herve* results in an intermediate layer that is thermodynamically unstable (i.e. the amorphous layer will recrystallize above ~400°C in the case of Si) which is likely inapplicable to high frequency applications.

Inoue is directed to transferring a thin film device from one substrate to another by use of a separation layer. Furthermore, as noted, *Inoue*'s re-crystallisation is used to generate a silicon layer that can be used to make what may be a poor quality transistor that is likely not applicable to high frequency applications.

Thus, there is no teaching or suggestion in the combination of references that would lead one of ordinary skill in the art to arrive at the claimed invention because of the differences between the combination and the claimed invention and the advantages realized by the claimed invention.

The combination of *Auberton-Herve*, *AAPA* and *Inoue* does not render the claimed invention *prima facie* obvious.

Withdrawal of the rejection of claims 25 and 26 is respectfully requested.

6. Claim 34.

Claim 34 is not rejected in view of any prior art.

At least claim 34 should be indicated as allowable in the next Official Action.

7. New Claims.

New claims 39-61 recite further inventive features. For example, independent claims 45 and 56 include the feature of the intermediate layer being in contact with

the silicon substrate and the insulating layer. These claims and their dependent claims define a three layer structure whereas *Auberton-Herve* uses a four layer structure.

Accordingly, claims 39-61 are believed to be allowable over the combination of *Auberton-Herve*, *AAPA* and *Inoue*.

8. Conclusion.

As a result of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is respectfully requested that every pending claim in the present application be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's attorney, the Examiner is invited to contact the undersigned at the numbers shown below.

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Respectfully submitted,

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